

**What is claimed is:**

1. A method of fabricating a thin silicon-on-insulator device comprising:
  - providing a structure having at least a first device region and a second device region, each device region comprising at least one gate region located on a SOI layer, said at least one gate region having exposed sidewalls;
  - forming a set of thin spacers on said exposed sidewalls of said each gate region;
  - forming raised source/drain regions on said SOI layer adjacent to said each gate region;
  - blocking said second device region with a block mask and implanting dopants of a first conductivity type into said raised source/drain regions in said first device region to form a first dopant impurity region;
  - removing the block mask from the second device region;
  - blocking said first device region with another block mask and implanting dopants of a second conductivity type into said raised source/drain region in said second device region to form a second dopant impurity region;
  - removing said another block mask; and

activating said first dopant impurity region and said second dopant impurity region.

2. The method of Claim 1 wherein said structure comprises a silicon-on-insulator substrate having a layer of semiconducting material atop an insulating layer.

3. The method of Claim 2 wherein said layer of semiconducting material is a Si containing material.

4. The method of Claim 2 wherein said layer of semiconducting material has a thickness of less than about 200 Å.

5. The method of Claim 1 wherein each of said thin spacers has a width of about 3.0 nm to about 15.0 nm.

6. The method of Claim 2 wherein said raised source/drain regions in said first device region and said second device region are formed by a selective epitaxial growth process.

7. The method of Claim 1 wherein a hard mask structure is used to pattern said at least one gate region and prevent epitaxial growth atop said at least one gate region during formation of said raised source/drain regions.

8. The method of Claim 1 wherein said block mask of said first device region and said another block mask of said second device region are a patterned photoresist.
9. The method of Claim 1 further comprising forming a set of offset spacers abutting said set of thin spacers, prior to forming said first dopant impurity region.
10. The method of Claim 9 wherein each spacer of said set of offset spacers has a thickness from about 2 nm to about 15 nm.
11. The method of Claim 9 wherein a set of second offset spacers is formed adjacent said set of offset spacers, prior to forming said dopant impurity region.
12. The method of Claim 11 wherein a second spacer of said set of second offset spacers has a thickness from about 2 nm to about 15 nm.
13. The method of Claim 1 wherein said activating said first dopant impurity region and said second dopant impurity region comprises annealing.
14. The method of Claim 13 wherein said annealing said first dopant impurity region and said second dopant impurity region forms a first dopant diffusion region underlying said raised source/drain region in said first device region and second dopant diffusion region underlying said raised source/drain region in said second device region.

15. The method of Claim 1 wherein said dopants of said first conductivity type comprise group V elements.

16. The method of Claim 1 wherein said dopants of said second conductivity type comprise group III-A element.

17. A thin channel silicon-on-insulator device comprising:

a substrate having a layer of semiconducting material atop an insulating layer;

a gate region atop said layer of semiconducting material;

a set of thin spacers abutting said gate region having a first spacer width;

a raised source/drain region on either side of said channel and atop said layer of semiconducting material, wherein said raised source/drain region are separated from said gate region by said set of thin spacers; and

a set of offset spacers having a offset spacer width atop said raised source/drain region and adjacent said set of thin spacers, wherein said offset spacer width is greater than said thin spacer width.

18. The thin channel silicon-on-insulator device of Claim 17 wherein said thin spacer width ranges from about 3.0 nm to about 15.0 nm.
19. The thin channel silicon-on-insulator device of Claim 17 further comprising extension regions underlying said thin spacer.
20. The thin channel silicon-on-insulator device of Claim 19 further comprising halo regions located underneath and laterally adjacent to said extension regions.